

# ***HHW microSD Card***

## **SD3.0 UHS-I**

### ***Datasheet***

**Rev. 1.0**

杭州瀚海微科技有限公司

## REVISION HISTORY

| Revision | Description                  | Date            |
|----------|------------------------------|-----------------|
| V1.1     | First released               | August, 2015    |
| V1.2     | Updated humidity information | March, 2017     |
| V1.3     | Part number updated          | September, 2018 |
|          |                              |                 |

### 1. Product Introduction

#### 1.1. Overview

The microSD Card is designed for demanding industrial applications. The microSD Card is compatible with SD 3.0 and provides excellent performance. The built-in auto ECC function can detect and correct errors during data transfer. Moreover, the Industrial microSD Card supports Ultra High Speed (UHS) interface transfer mode, provides high write/read data transfer rate, sudden Power-Fails protection, adaptive static wear-leveling, read/program disturb management, etc. It was designed to meet the high quality, high reliability, high performance, and versatile environmental requirements.

#### 1.2. Product Features

- Interface: 8 pins microSD standard interface
- Compliant SD Card Specification 3.0
- Density support:
  - MLC: 4GB~32GB
  - TLC: 64-128GB
- Bus Speed Mode:
  - DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR12: 1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
  - SDR25: 1.8V signaling, frequency up to 50MHz, up to 25MB/sec
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50MB/sec

- SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
- DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/s
- Operating Temperature: N-Temp: at 0°C to 70°C
- Flash: MLC NAND Flash
- Read disturbance management
- Adaptive wear leveling

## 2. microSD Card Interface Description

### 2.1 microSD Pin Assignment

**Table 1: microSD Bus Mode Pin Definition**

| Pin # | Name    | Type | microSD Description           |
|-------|---------|------|-------------------------------|
| 1     | DAT2    | I/O  | Data Line [Bit 2]             |
| 2     | CD/DAT3 | I/O  | Card Detect / Data Line[Bit3] |
| 3     | CMD     | PP   | Command / Response            |
| 4     | VDD     | S    | Supply Voltage                |
| 5     | CLK     | I    | Clock                         |
| 6     | VSS     | S    | Supply Voltage Ground         |
| 7     | DAT0    | I/O  | Data Line [Bit 0]             |
| 8     | DAT1    | I/O  | Data Line [Bit 1]             |

Notes:

- 1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
- 2) The extended DAT Lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET\_BUS\_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to Multi-media Cards.
- 3) After power up this line (Pin2) is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by user, during regular data transfer, with SET\_CLR\_CARD\_DETECT (ACMD42) command.

**Table 2: SPI Bus Mode Pin Definition**

| Pin # | Name | Type | microSD Description    |
|-------|------|------|------------------------|
| 1     | RSV  |      | Reserved               |
| 2     | CS   | I    | Chip Select (neg true) |
| 3     | DI   | I    | Data In                |
| 4     | VDD  | S    | Supply Voltage         |
| 5     | SCLK | I    | Clock                  |
| 6     | VSS  | S    | Supply Voltage Ground  |
| 7     | DO   | O    | Data Out               |

|   |     |  |          |
|---|-----|--|----------|
| 8 | RSV |  | Reserved |
|---|-----|--|----------|

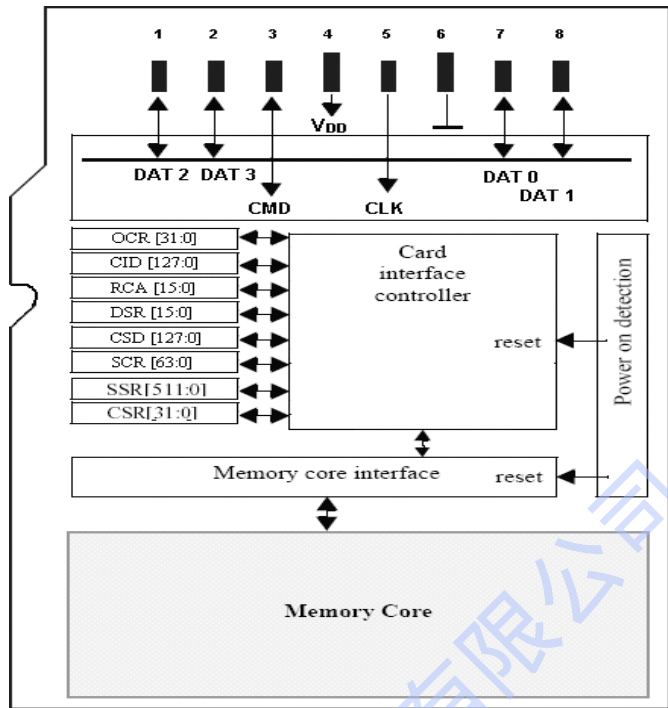


Figure 1: Functional Diagram

### 3. Specifications

#### 3.1. Performance

Max. Data Transfer Rate

- Read: 90MB/s; Write: 70MB/s

#### 3.2. NAND Flash Memory

microSD Card Multi Level Cell (MLC) and (TLC) NAND Flash memory, which is non-volatility, high reliability and high speed memory storage.

#### 3.3. Power Requirement

##### 3.3.1. DC Input Voltage

- 2.7V to 3.6V

#### 3.4. Temperature Range

- N-Temp: 0°C to 70°C

#### 3.5. Humidity

Relative Humidity: 5-95%, non-condensing

### 4. Electrical Specifications

#### 4.1. General DC Characteristic

W-Temp

Table 3: Absolute Maximum Ratings

| Symbol               | Parameter                     | Min. | Max. | Unit | Note |
|----------------------|-------------------------------|------|------|------|------|
| T <sub>storage</sub> | Storage Temperature           | -25  | 95   | °C   | -    |
| T <sub>a</sub>       | Ambient Operating Temperature | 0    | 85   | °C   | -    |
| V <sub>I</sub>       | 3.3V External Input Voltage   | -0.3 | 3.6  | V    | -    |

N-Temp

| Symbol               | Parameter                     | Min. | Max. | Unit | Note |
|----------------------|-------------------------------|------|------|------|------|
| T <sub>storage</sub> | Storage Temperature           | -25  | 85   | °C   | -    |
| T <sub>a</sub>       | Ambient Operating Temperature | 0    | 85   | °C   | -    |
| V <sub>I</sub>       | 3.3V External Input Voltage   | -0.3 | 3.6  | V    | -    |

Table 4: Power Consumption

| Symbol      | Parameter               | Min. | Typ. | Max. | Unit |
|-------------|-------------------------|------|------|------|------|
| $I_{Read}$  | Read Current at 3.3V    | -    | 169  | -    | mA   |
| $I_{Write}$ | Write Current at 3.3V   | -    | 89   | -    | mA   |
| $I_{STBY}$  | Standby Current at 3.3V | -    | 198  | -    | uA   |

## 4.2. Bus Operation Conditions for 3.3V Signaling

### 4.2.1 Threshold Level for High Voltage Range

**Table 5: Threshold Level for High Voltage**

| Parameter           | Symbol   | Min                  | Max                  | Unit | Remark                      |
|---------------------|----------|----------------------|----------------------|------|-----------------------------|
| Supply Voltage      | $V_{DD}$ | 2.7                  | 3.6                  | V    |                             |
| Output High Voltage | $V_{OH}$ | $0.75 \cdot V_{DD}$  |                      | V    | $I_{OH}=2mA \ V_{DD \ min}$ |
| Output Low Voltage  | $V_{OL}$ |                      | $0.125 \cdot V_{DD}$ | V    | $I_{OL}=2mA \ V_{DD \ min}$ |
| Input High Voltage  | $V_{IH}$ | $0.625 \cdot V_{DD}$ | $V_{DD}+0.3$         | V    |                             |
| Input Low Voltage   | $V_{IL}$ | $V_{ss}-0.3$         | $0.25 \cdot V_{DD}$  | V    |                             |
| Power Up Time       |          |                      | 250                  | ms   | From 0V to $V_{DD \ min}$   |

### 4.2.2 Peak Voltage and Leakage Current

**Table 6: Peak Voltage and Leakage Current**

| Parameter                 | Symbol | Min  | Max          | Unit | Remark |
|---------------------------|--------|------|--------------|------|--------|
| Peak voltage on all lines |        | -0.3 | $V_{DD}+0.3$ | V    |        |
| All Inputs                |        |      |              |      |        |
| Input Leakage Current     |        | -10  | 10           | uA   |        |
| All Outputs               |        |      |              |      |        |
| Output Leakage Current    |        | -10  | 10           | uA   |        |

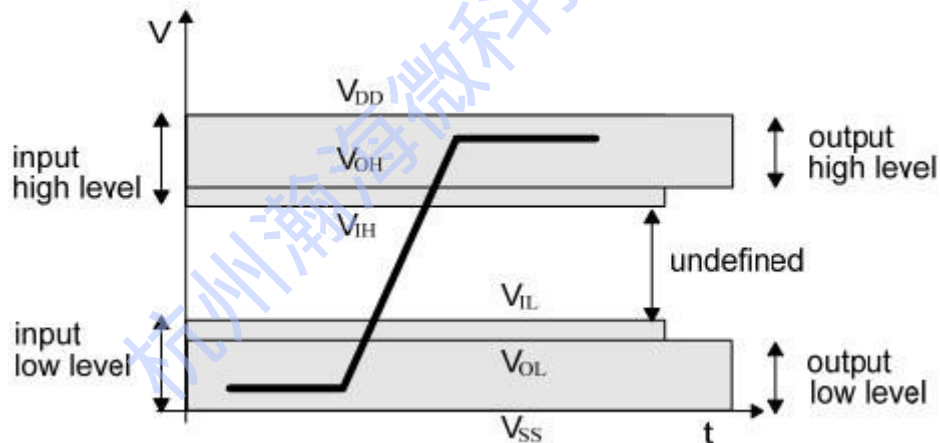
### 4.2.3 Bus Signal Line Load

**Table 7: Bus Operating Conditions - Signal Line's Load**

| Parameter                                  | Symbol                 | Min | Max | Unit       | Remark                                          |
|--------------------------------------------|------------------------|-----|-----|------------|-------------------------------------------------|
| Pull-up resistance                         | $R_{CMD}$<br>$R_{DAT}$ | 10  | 100 | K $\Omega$ | To prevent bus floating                         |
| Total bus capacitance for each signal line | $C_L$                  |     | 40  | pF         | 1 card $C_{HOST}+C_{BUS}$ shall not exceed 30pF |
| Card capacitance for each signal pin       | $C_{CARD}$             |     | 10  | pF         |                                                 |
| Maximum signal inductance                  |                        |     | 16  | nH         |                                                 |
| Pull-up resistance inside card(pin1)       | $R_{DAT3}$             | 10  | 90  | K $\Omega$ | May be used for card detection                  |
| Capacity Connected to Power Line           | $C_C$                  |     | 5   | $\mu$ F    | To prevent inrush current                       |

### 4.2.4 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



**Figure 2: Bus Signal Levels**

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 6 for any VDD of the allowed voltage range.

#### 4.2.5 Bus Timing (Default)

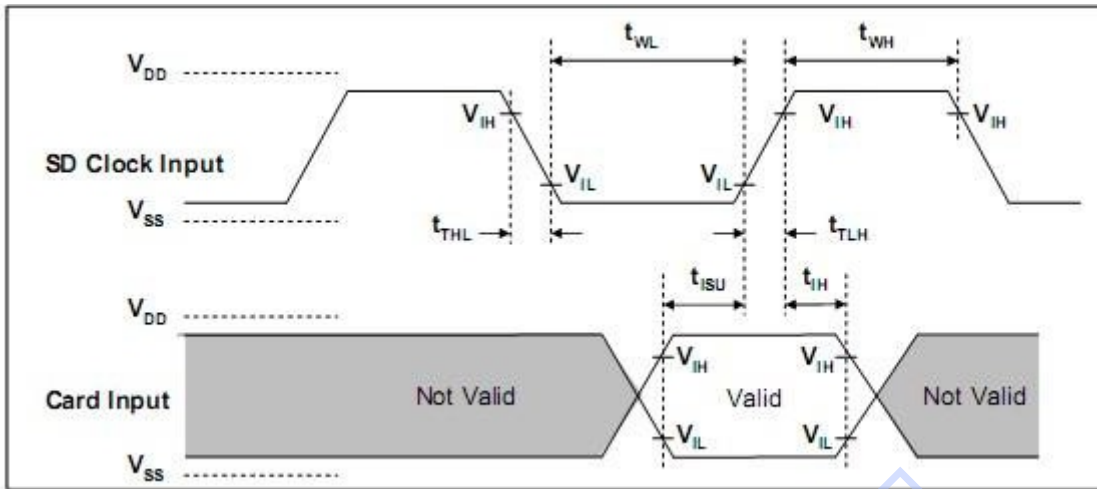


Figure 3: Card input Timing (Default Speed Card)

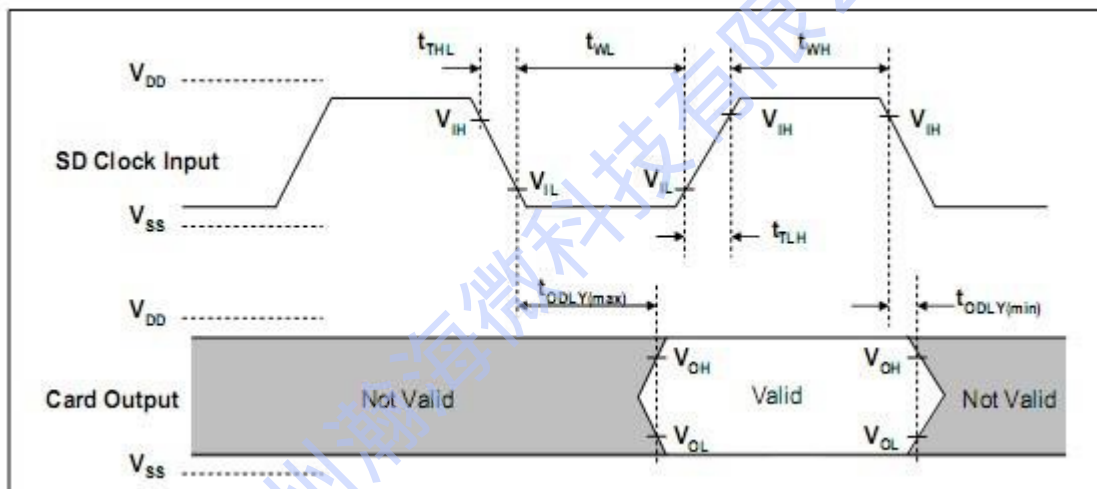


Figure 4: Card Output Timing (Default Speed

Mode) Table 8: Bus Timing-Parameters Values

| Parameter                                                                           | (Default Speed) | Symbol           | Min.                  | Max | Unit | Remark                        |
|-------------------------------------------------------------------------------------|-----------------|------------------|-----------------------|-----|------|-------------------------------|
| <b>Clock CLK</b> ( All values are referred to min ( $V_{IH}$ ) and max ( $V_{IL}$ ) |                 |                  |                       |     |      |                               |
| Clock frequency data transfer                                                       |                 | fpp              | 0                     | 25  | MHz  | $C_{CARD} \leq 10pF$ (1 card) |
| Clock frequency Identification                                                      |                 | f <sub>OD</sub>  | 0 <sup>(1)</sup> /100 | 400 | KHz  | $C_{CARD} \leq 10pF$ (1 card) |
| Clock low time                                                                      |                 | t <sub>WL</sub>  | 10                    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock high time                                                                     |                 | t <sub>WH</sub>  | 10                    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock rise time                                                                     |                 | t <sub>TLH</sub> |                       | 10  | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock fall time                                                                     |                 | t <sub>THL</sub> |                       | 10  | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| <b>Inputs CMD, DAT</b> (referenced to CLK)                                          |                 |                  |                       |     |      |                               |
| Input set-up time                                                                   |                 | t <sub>ISU</sub> | 5                     |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |

|                                             |            |   |    |    |                               |
|---------------------------------------------|------------|---|----|----|-------------------------------|
| Input hold time                             | $t_{TH}$   | 5 |    | ns | $C_{CARD} \leq 10pF$ (1 card) |
| <b>Outputs CMD, DAT (referenced to CLK)</b> |            |   |    |    |                               |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | 0 | 14 | ns | $C_L \leq 40pF$ (1 card)      |
| Output Hold time                            | $t_{OH}$   | 0 | 50 | ns | $C_L \leq 40pF$ (1 card)      |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required (refer to Chapter 4.4-Clock Control)

#### 4.2.6 Bus Timing (High-Speed Mode)

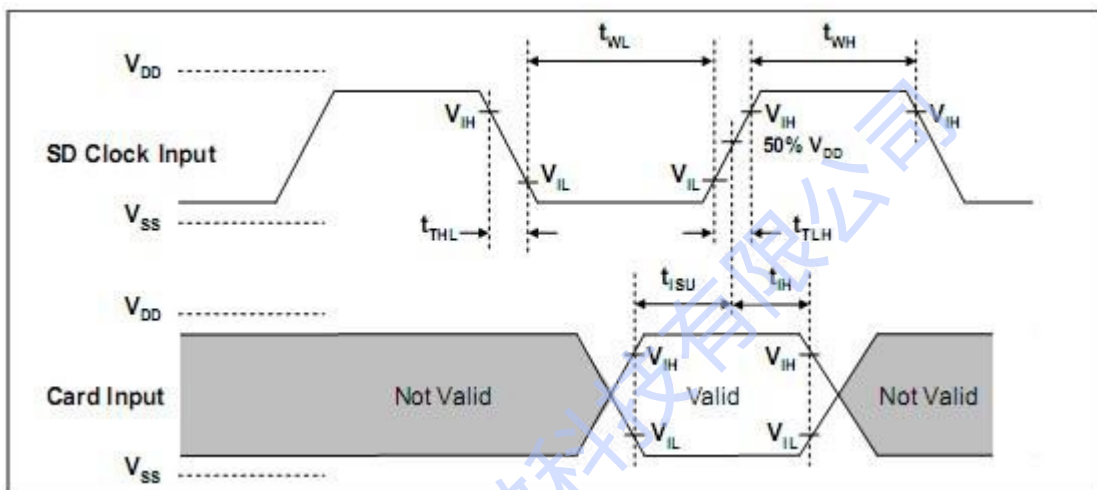


Figure 5: Card Input Timing (High Speed Card)

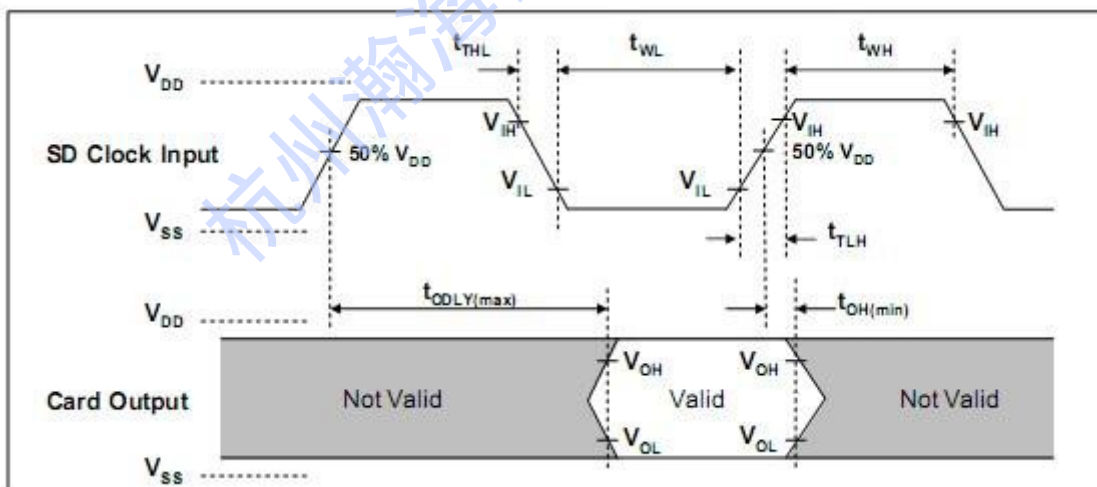


Figure 6: Card Output Timing (High Speed Mode)

**Table 9 : Bus Timing – Parameters Values(High Speed)**

| Parameter                                                                             | Symbol     | Min. | Max | Unit | Remark                        |
|---------------------------------------------------------------------------------------|------------|------|-----|------|-------------------------------|
| <b>Clock CLK</b> ( All values are referred to min ( $V_{IH}$ ) and max ( $V_{IL}$ ) ) |            |      |     |      |                               |
| Clock frequency data transfer                                                         | fpp        | 0    | 50  | MHz  | $C_{CARD} \leq 10pF$ (1 card) |
| Clock low time                                                                        | $t_{WL}$   | 7    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock high time                                                                       | $t_{WH}$   | 7    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock rise time                                                                       | $t_{TLH}$  |      | 3   | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Clock fall time                                                                       | $t_{THL}$  |      | 3   | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| <b>Inputs CMD, DAT</b> (referenced to CLK)                                            |            |      |     |      |                               |
| Input set-up time                                                                     | $t_{ISU}$  | 6    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| Input hold time                                                                       | $t_{TH}$   | 2    |     | ns   | $C_{CARD} \leq 10pF$ (1 card) |
| <b>Outputs CMD, DAT</b> (referenced to CLK)                                           |            |      |     |      |                               |
| Output Delay time during Data Transfer Mode                                           | $t_{ODLY}$ |      | 14  | ns   | $C_L \leq 40pF$ (1 card)      |
| Output Hold time                                                                      | $t_{OH}$   | 2.5  |     | ns   | $C_L \geq 15pF$ (1 card)      |
| Total System capacitance for each line <sup>1</sup>                                   | $C_L$      |      | 40  | pF   | 1 card                        |

1) In order to satisfy sever timing, host shall drive only one card.

### 4.3 Bus Operation Conditions for 1.8V Signaling

#### 4.3.1 Threshold Level for High Voltage Range

**Table 10: Threshold Level for High Voltage**

| Parameter           | Symbol     | Min          | Max  | Unit | Remark                    |
|---------------------|------------|--------------|------|------|---------------------------|
| Supply Voltage      | $V_{DD}$   | 2.7          | 3.6  | V    |                           |
| Regulator Voltage   | $V_{DDIO}$ | 1.7          | 1.95 | V    | Generated by $V_{DD}$     |
| Output High Voltage | $V_{OH}$   | 1.4          |      | V    | $I_{OH}=2mA$ $V_{DD}$ min |
| Output Low Voltage  | $V_{OL}$   |              | 0.45 | V    | $I_{OL}=2mA$ $V_{DD}$ min |
| Input High Voltage  | $V_{IH}$   | 1.27         | 2.0  | V    |                           |
| Input Low Voltage   | $V_{IL}$   | $V_{SS}-0.3$ | 0.58 | V    |                           |

#### 4.3.2 Peak Voltage and Leakage Current

**Table 11: Peak Voltage and Leakage Current**

| Parameter             | Symbol | Min | Max | Unit | Remark                       |
|-----------------------|--------|-----|-----|------|------------------------------|
| Input Leakage Current |        | -2  | 2   | uA   | DAT3 pull-up is disconnected |

### 4.3.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

#### 4.3.3.1 Clock Timing

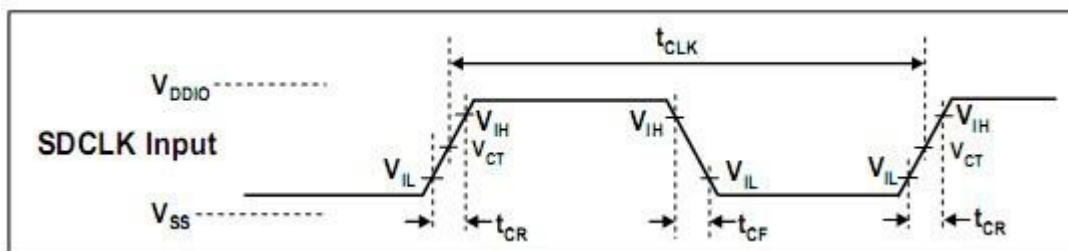


Figure 7: Clock Signal

Timing Table 12: Clock

| Symbol           | Min | Max             | Unit | Remark                                                                                                                                                                                                             |
|------------------|-----|-----------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{CLK}$        | 4.8 | -               | ns   | Signal Timing<br>208MHz (Max.), Between rising edge, $V_{CT}=0.975V$                                                                                                                                               |
| $t_{CR}, t_{CF}$ | -   | $0.2 * t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 2.00ns$ (max.) at 208MHz, $C_{CARD}=10pF$<br>$t_{CR}, t_{CF} < 2.00ns$ (max.) at 100MHz, $C_{CARD}=10pF$<br>The absolute maximum value of $t_{CR}, t_{CF}$ is 10ns regardless of clock frequency |
| Clock Duty       | 30  | 70              | %    |                                                                                                                                                                                                                    |

#### 4.3.3.2 Card Input Timing

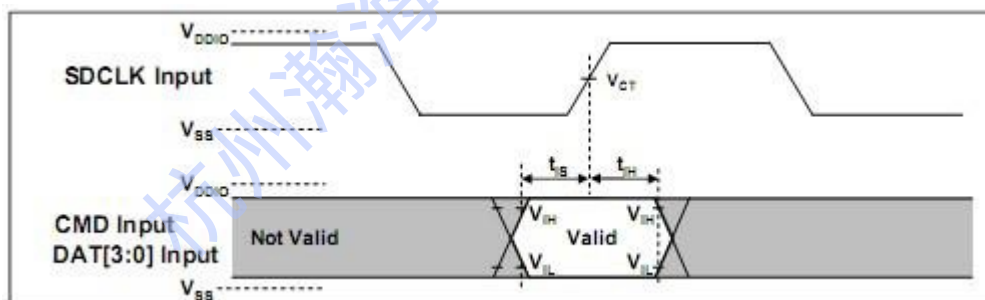


Figure 8: Card Input Timing

Table 13: SDR50 and SDR104 Input Timing

| Symbol   | Min  | Max | Unit | SDR104 mode                        |
|----------|------|-----|------|------------------------------------|
| $t_{IS}$ | 1.40 | -   | ns   | $C_{CARD} = 10pF, V_{CT} = 0.975V$ |
| $t_{IH}$ | 0.80 |     | ns   | $C_{CARD} = 5pF, V_{CT} = 0.975V$  |
| Symbol   | Min  | Max | Unit | SDR12, SDR25 and SDR50 modes       |
| $t_{IS}$ | 3.00 | -   | ns   | $C_{CARD} = 10pF, V_{CT} = 0.975V$ |
| $t_{IH}$ | 0.80 | -   | ns   | $C_{CARD} = 5pF, V_{CT} = 0.975V$  |

### 4.3.3.3 Card Output Timing

#### 4.3.3.3.1 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

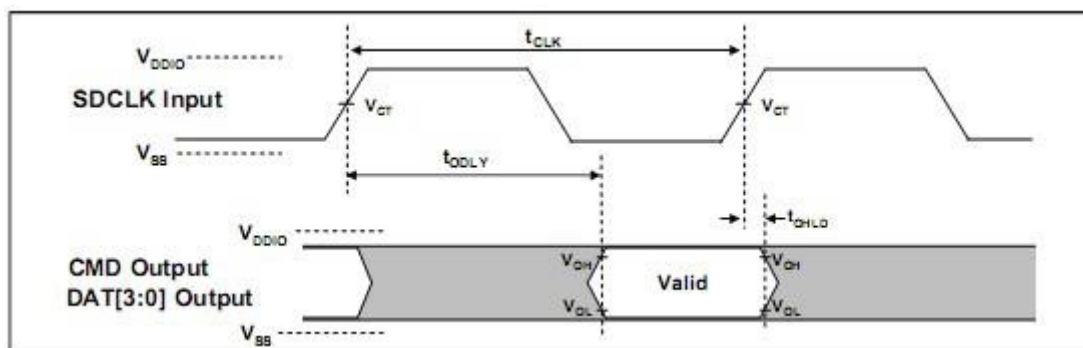


Figure 9: Output Timing of Fixed Date

Window Table 14: Output Timing of Fixed

Data Window

| Symbol     | Min | Max | Unit | Remark                                                                                      |
|------------|-----|-----|------|---------------------------------------------------------------------------------------------|
| $t_{ODLY}$ | -   | 7.5 | ns   | $t_{CLK} \geq 10.0\text{ns}$ , $CL=30\text{pF}$ , using driver Type B, for SDR50.           |
| $t_{ODLY}$ |     | 14  | ns   | $t_{CLK} \geq 20.0\text{ns}$ , $CL=40\text{pF}$ , using driver Type B, for SDR25 and SDR12. |
| $t_{OH}$   | 1.5 | -   | ns   | Hold time at the $t_{ODLY}$ (min.). $CL=15\text{pF}$                                        |

#### 4.3.3.3.2 Output Timing of Variable Window (SDR104)

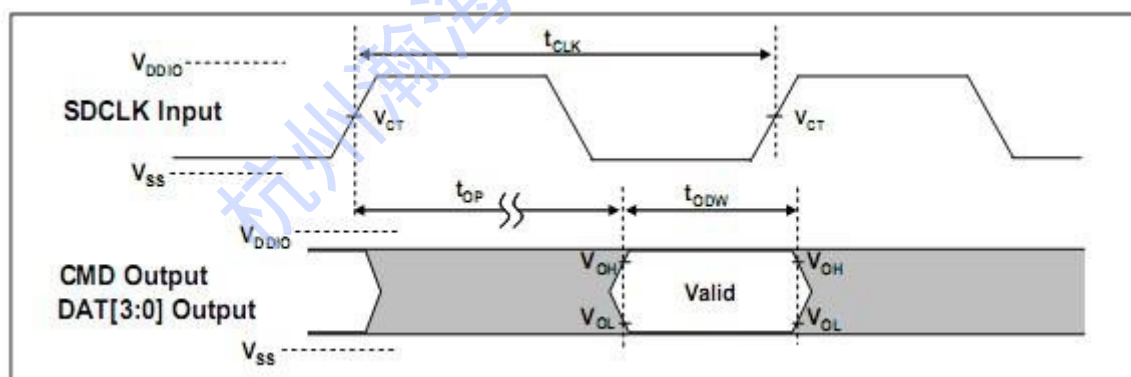


Figure 10: Output Timing of Variable Data

| Symbol          | Min  | Max | Unit | Remark                                                 |
|-----------------|------|-----|------|--------------------------------------------------------|
| $t_{OP}$        | -    | 2   | UI   | Card Output Phase                                      |
| $\Delta t_{OP}$ | -350 | 500 | ps   | Delay variation due to temperature change after tuning |
| $t_{ODW}$       | 0.60 | -   | UI   | $t_{ODW} = 2.88\text{ns}$ at 208MHz                    |

## 5. Mechanical Dimensions

The mechanical dimensions of Agrade Industrial microSD Card were basically followed the mechanical form factor definitions on microSD card specifications which constructed by SD card association.

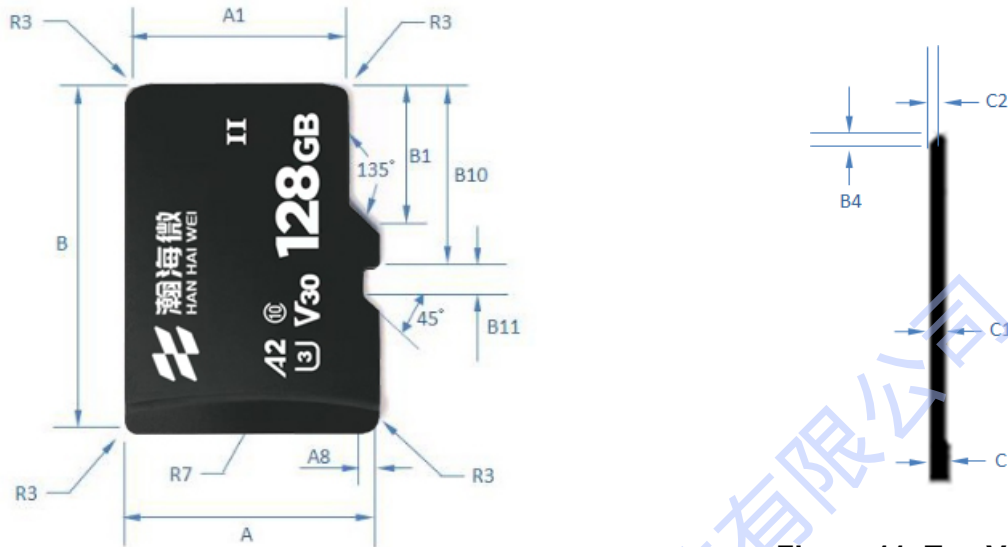


Figure 11: Top View  
Figure 12: Side View

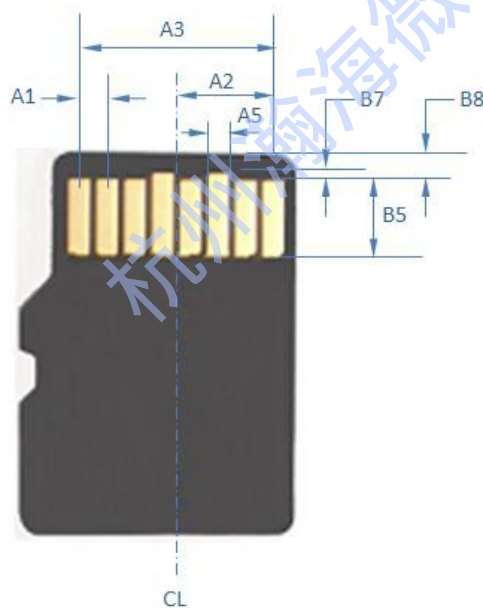


Figure 13: Bottom View

Criteria of microSD Unit: mm

| Dimensions | Min   | TYP   | Max   | Note  |
|------------|-------|-------|-------|-------|
| A          | 10.90 | 11.00 | 11.10 |       |
| A1         | 9.60  | 9.70  | 9.80  |       |
| A2         |       | 3.85  |       | BASIC |
| A3         | 7.60  | 7.70  | 7.80  |       |
| A4         |       | 1.10  |       | BASIC |
| A5         | 0.75  | 0.80  | 0.85  |       |
| A8         | 0.60  | 0.70  | 0.80  |       |
| B          | 14.90 | 15.00 | 15.10 |       |
| B1         | 6.13  | 6.23  | 6.33  |       |
| B4         | 0.42  | 0.52  | 0.62  |       |
| B5         | 2.80  | 2.90  | 3.00  |       |
| B7         | 0.20  | 0.30  | 0.40  |       |
| B8         | 1.00  | 1.10  | 1.20  |       |
| B10        | 7.80  | 7.90  | 8.00  |       |
| B11        | 1.10  | 1.20  | 1.30  |       |
| R3         | 0.70  | 0.80  | 0.90  |       |
| R7         | 29.50 | 30.00 | 30.50 |       |
| C          | 0.90  | 1.00  | 1.10  |       |
| C1         | 0.60  | 0.70  | 0.80  |       |
| C2         | 0.20  | 0.30  | 0.40  |       |

## 6. Ordering Information

|          | microSD Card(MLC)  | microSD Card( SLC) |
|----------|--------------------|--------------------|
| Capacity | Normal-temperature | Wide-temperature   |
| 4GB      | HHW4GTFC-BC10      |                    |
| 8GB      | HHW8GTFC-BC10      |                    |
| 16GB     | HHW16GTFC-BC10     |                    |
| 32GB     | HHW32GTFC-BC10     |                    |

| microSD Card(TLC) |                    |                      |                  |
|-------------------|--------------------|----------------------|------------------|
| Capacity          | Normal-Temperature | Extended-Temperature | Wide-temperature |
| 4GB               |                    |                      |                  |
| 8GB               |                    |                      |                  |
| 16GB              |                    |                      |                  |
| 32GB              |                    |                      |                  |
| 64GB              | HHW64GTFC-BU3      |                      |                  |
| 128GB             | HHW128GTFC-BU3     |                      |                  |