SD NAND SPECIFICATION

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1. Overview

1.1 Product Description

Hanhai-tech SD NAND are highly integrated flash memories with serial and random access capability. Can be use in the device which can support SD2.0 standard. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission.

The purpose of product development is to make memory chips based on SD interface more stable and use scenarios more abundant. Han hai-tech SD NAND can match more MCUS with stable quality and strong compatibility, and can perfectly replace the previous storage products based on SDIO interface. The low power consumption of the product itself is more suitable for handheld products, and the rigorous production process makes the product more suitable for diverse scenarios

1.2 Features Summary

-Capacity: 8GB/16GB
-Complies to SD Specification 3.0
-Supports SD & SPI Mode
-Voltage range for communication: 2.7~3.6V
-Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance)
-Up to 25 MB/sec data transfer rate (using four parallel data lines)
-password protection (CMD42-LOCK_UNLOCK)
-Sophisticated system for error recovery including a powerful ECC
-Global Wear Leveling
-Bad block management;
-Program/Erase:20000cycles
-Power management for low power operation

2. Pin Assignment

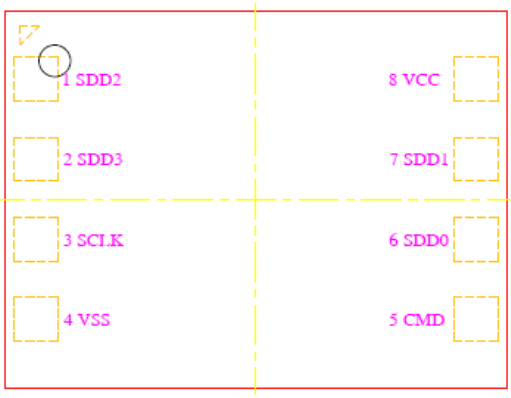


Figure 1:Top View

	SD Mode		SPI Mode	
Name	**Tyte**	**Description**	**Tyte**	**Description**
DAT2	I/O/PP	Data Line [Bit2]	RSV	Reserved
DAT3	I/O/PP	Data Line [Bit3]	I3	Chip select(neg true)
CLK	I	Clock	I	Clock
GND	S	Supply voltage ground	S	Supply voltage ground
VDD	S	Supply voltage	S	Supply voltage
DAT1	I/O/PP	Data Line [Bit1]	RSV	Reserved
DAT0	I/O/PP	Data Line [Bit0]	OPP	Data Out
CMD	PP	Command/Response	I	Data In

Table 1: Pin Assignment

3. Product List

Product model	Capacity	Actual Size	Sequential R/W	Package
HHW64GS90I-D1	8GB	7360MB	10/20MB/S	9*13 (mm)
HHW128GS90I-D1	16GB	14550MB	10/20MB/S	9*13 (mm)

Table 2: Product List

4. Current Consumption

Standby current: 250uA (Maximum value)

Standby current: 200uA (average value)

Operating current: 95mA (Maximum value)

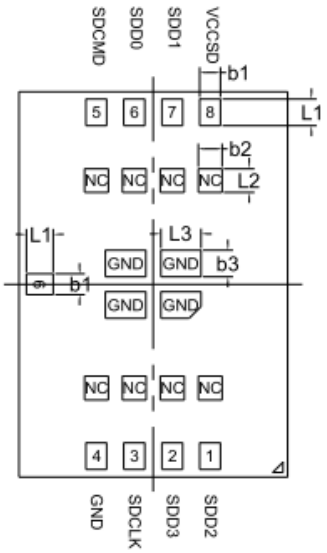
Operating current: 80mA (average value)

5. Operational Environment

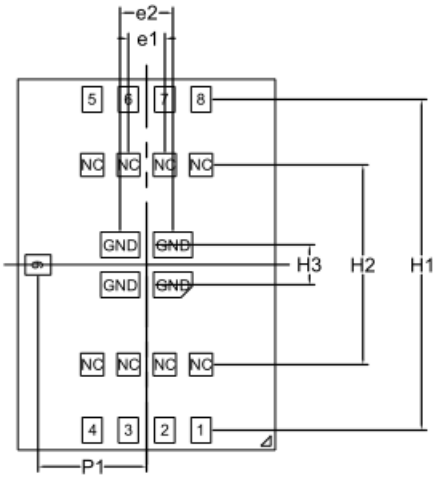
Parameter	Range	
Temperature	Operating	-25℃~85℃
	Non-Operating	-50℃~150℃
Humidity	Operating	25% to 85%, non-condensing
	Non-Operating	25% to 85%, non-condensing
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]	

Table 3: Operational Environment

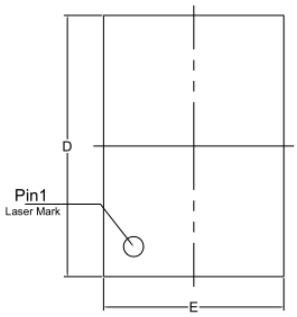
6. Physical Dimension



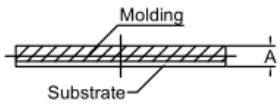
Bottom View



Bottom View



TOP View



Side View

SYMBOL	DIMENSION IN MM			DIMENSION IN MIL		
	Min.	Nor.	Max.	Min.	Nor.	Max.
D	12.90	13.00	13.10	507.87	511.81	515.75
E	8.90	9.00	9.10	350.39	354.33	358.27
b1	0.65	0.70	0.75	25.59	27.56	29.53
b2	0.75	0.80	0.85	29.53	31.50	33.46
b3	0.85	0.90	0.95	33.46	35.43	37.40
L1	0.85	0.90	0.95	33.46	35.43	37.40
L2	0.75	0.80	0.85	29.53	31.50	33.46
L3	1.30	1.35	1.40	51.18	53.15	55.12
e1	/	1.27 Typ.	/	/	50.00 Typ.	/
e2	/	1.85 Typ.	/	/	72.84 Typ.	/
P1	/	3.80 Typ.	/	/	149.61 Typ.	/
H1	/	11.35 Typ.	/	/	447.24 Typ.	/
H2	/	6.85 Typ.	/	/	269.68 Typ.	/
H3	/	1.40 Typ.	/	/	55.12 Typ.	/
A	0.75	0.80	0.85	29.53	31.50	33.46

7. Recommended Schematic

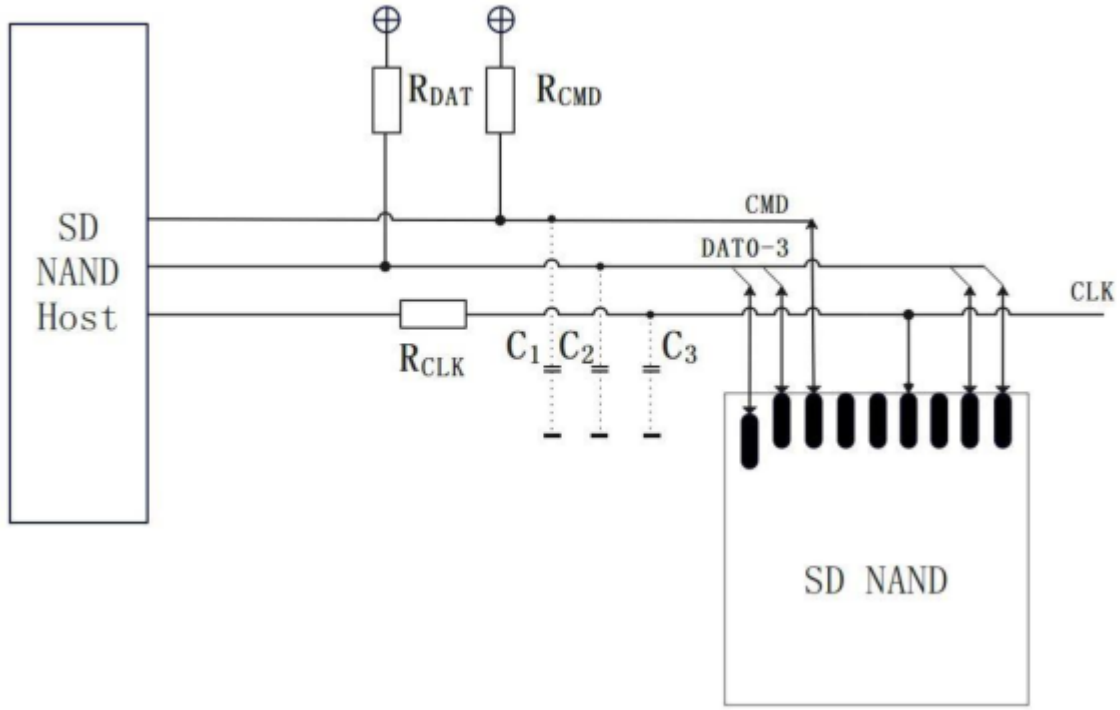


Figure 4: Recommended Schemati

Note:
Rdat and Rcmd (10K-100kΩ) are pull-up resistors protecting the CMD and the DAT lines against bus floating when SDNAND is in a high-impedance mode.
The host shall pull-up all DAT0-3 lines by Rdat. even if the host uses the SDNAND as 1-bit mode only in SD mode. It is recommended to have 2.2uF capacitance on VCC
Rclk reference 0~120Ω

8. Commands

Command Types
There are four kinds of commands defined to control the SD Memory Card:

• Broadcast commands (bc), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated, then each card will accept it separately in its turn.

• Broadcast commands with response (bcr) response from all cards simultaneously - Since there is no Open Drain mode in SD Memory Card, this type

of command shall be used only if all the CMD lines are separated - the command will be accepted and responded by every card separately.

- Addressed (point-to-point) commands (ac) no data transfer on DAT
- Addressed (point-to-point) data transfer commands (adtc) data transfer on DAT

All commands and responses are sent over the CMD line of the SD Memory Card. The command transmission always starts with the left bit of the bit string corresponding to the command codeword.

Command Format

All commands have a fixed code length of 48 bits, needing a transmission time of 1.92 μs @ 25 MHzand 0.96 μs @ 50 MHz.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width(bits)	1	1	6	32	7	1
Value	"0"	"1"	x	x	x	"1"
Description	Start bit	Transmission bit	Command index	Argument	CRC7	End bit

Command Classes

The command set of the SD Memory Card system is divided into several classes. Each class supports a set of card functionalities.determines the setting of CCC from the card supported commands. A CCC bit, which corresponds to a supported command number, is set to 1. A class in CCC includes mandatory commands is always set to 1. Cards with specific functions may need to support some optional commands. For example, Combo Card shall support CMD5.

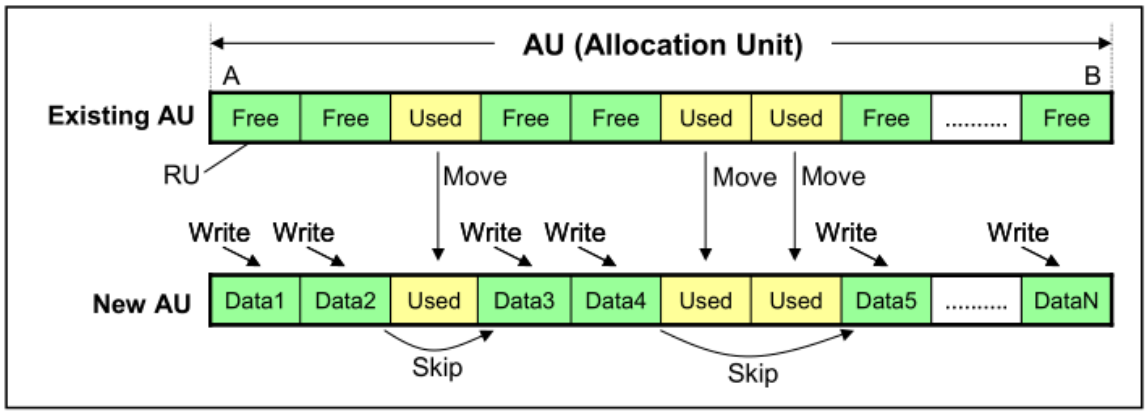
Class 0, 2, 4, 5 and 8 are mandatory and shall be supported by all SD Memory Cards. Class 7 except CMD40 is mandatory for SDHC and SDXC. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each card, providing the host with information on how to access the card.

Card Command Class (CCC)		0	1	2	3	4	5	6	7	8	9	10	11
Supported commands	class description	basic	reserved	block read	reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD2	Mandatory	+											
CMD3	Mandatory	+											
CMD4	Mandatory	+											
CMD5	Optional										+		
CMD6[2]	Mandatory											+	
CMD7	Mandatory	+											
CMD8[3]	Mandatory	+											
CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD11[5]	Optional	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD15	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD19[5]	Optional			+									
CMD20[6]	Optional			+		+							
CMD23[7]	Optional			+		+							
CMD24[1]	Mandatory					+							
CMD25[1]	Mandatory					+							
CMD27[1]	Mandatory					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32[1]	Mandatory						+						
CMD33[1]	Mandatory						+						
CMD34-37[2]	Optional											+	
CMD38[1]	Mandatory						+						
CMD40	Optional								+				
CMD42[4]	(Note 4)								+				
CMD50[2]	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			

CMD56	Mandatory									+			
CMD57[2]	Optional											+	
ACMD6	Mandatory									+			
ACMD13	Mandatory									+			
ACMD22[1]	Mandatory									+			
ACMD23[1]	Mandatory									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

9. Write Performance

Below table shows the typical data management of the card when the host writes RUs of an AU. When the host writes to a fragmented AU, the card prepares a new AU by copying the used RUs and writing the new RUs.. The location A is at the start of the AU boundary and location B is at the end of the AU boundary. From A to B, the host shall write data to free RUs contiguously and skip used RUs (shall not skip any free RU). The card may indicate busy to the host, so the host can wait, during the time the card controller is writing and moving data. The total write time from A to B can be calculated by summing up the write time of free RUs and the moving time of the used RUs. The number of used RUs (Nu) is available by counting it over one AU and number of free RUs is expressed by (N RU – Nu).



Example of Writing Fragmented AU

The Performance Write (Pw) is defined as a minimum average write performance over an AU. It is calculated by taking the average of all sequential RU write operations to one complete AU, which is not fragmented.

The Performance Move (Pm) is defined as a minimum average move performance. It is calculated by taking the average over sequential RU move operations to one complete AU. A move is an internal operation of the card, so SD clock frequency does not affect the time of the move operation. In case the card does not have to move RU, Pm should be considered as infinity (1/Pm = 0).

Note that a Speed Class that supports Class10 shall not use the Pm value stored in the SD Status to calculate performance in any fragmented AU. Class 10 performance is defined only for entirely free AUs.

10. Read Performance

Two kinds of read performances are defined. It is possible to insert either type of read operation during write operations. All read operations, regardless of read address shall meet this performance specification.

(1) Read Performance of Stream Data
This is simply called **Read Performance (Pr). Pr** is defined as minimum average random RU read performance. The average is measured over 256 random single RU read operations. Each RU is read by a multiple-read command. Pr shall be greater than or equal to Pw.

(2) FAT and Directory Entry Read Time
T_{FR}(4KB) is defined as the maximum time to read a 4KB FAT and Directory Entry. The **FAT and Directory Entry Read Time** (**S_{FR} [KB]**) is defined using the CEIL function:

FAT Read Time of S_{FR} [KB]: $$T_{FR}(S_{FR}) = \left\lceil \frac{S_{FR}}{4KB} \right\rceil \cdot T_{FR}(4KB) \quad \text{.....(2)}$$

(: CEIL function - Convert decimal fraction x to the smallest integer greater than or equal to x.)

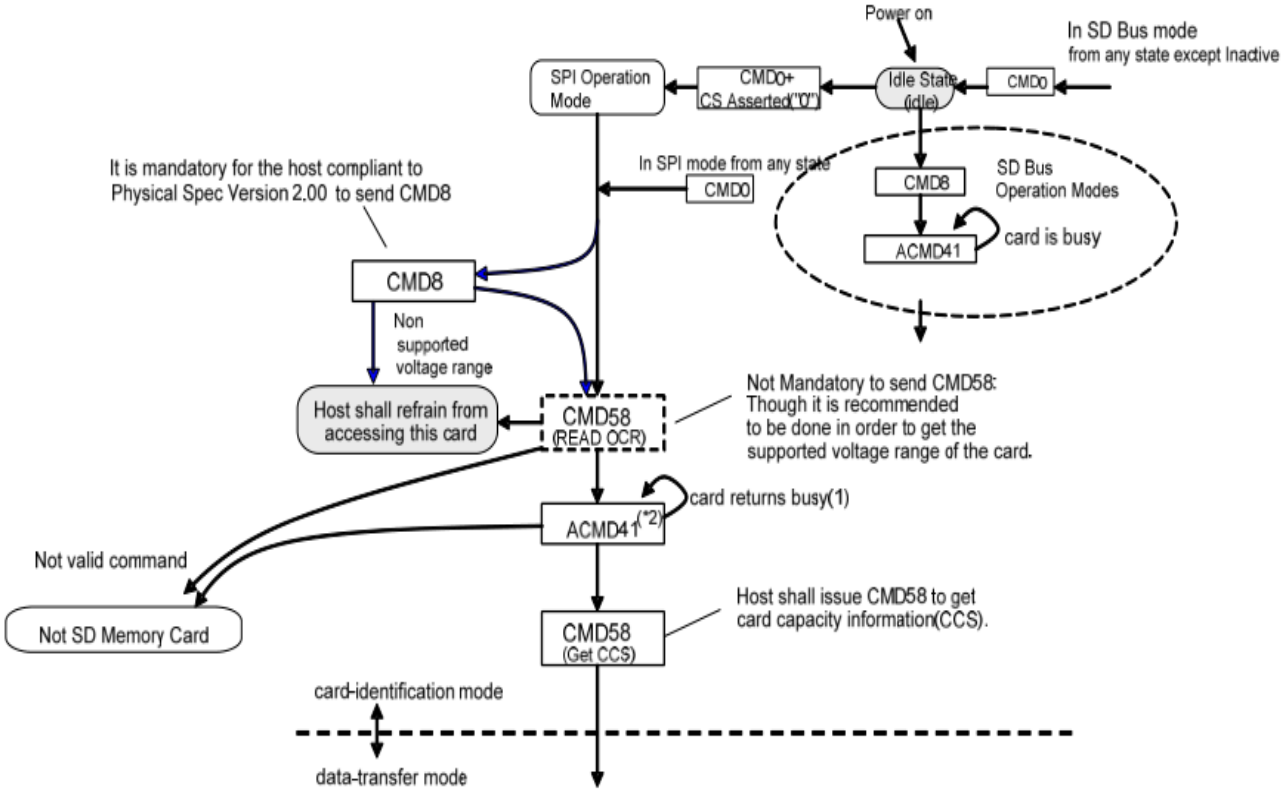
11. SPI Mode

The SPI mode consists of a secondary communication protocol that is offered by Flash-based SD Memory Cards. This mode is a subset of the SD Memory Card protocol, designed to communicate with a SPI channel, commonly found in Motorola's (and lately a few other vendors') micro controllers. The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses a subset of the SD Memory Card protocol and command set.

The advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance of the SPI mode versus SD mode (e.g. Single data line and hardware CS signal per card).

The commands and functions in SD mode defined after the Version 2.00 are not supported in SPI mode. The card may respond to the commands and functions even if the card is in SPI mode but host should not use them in SPI mode.

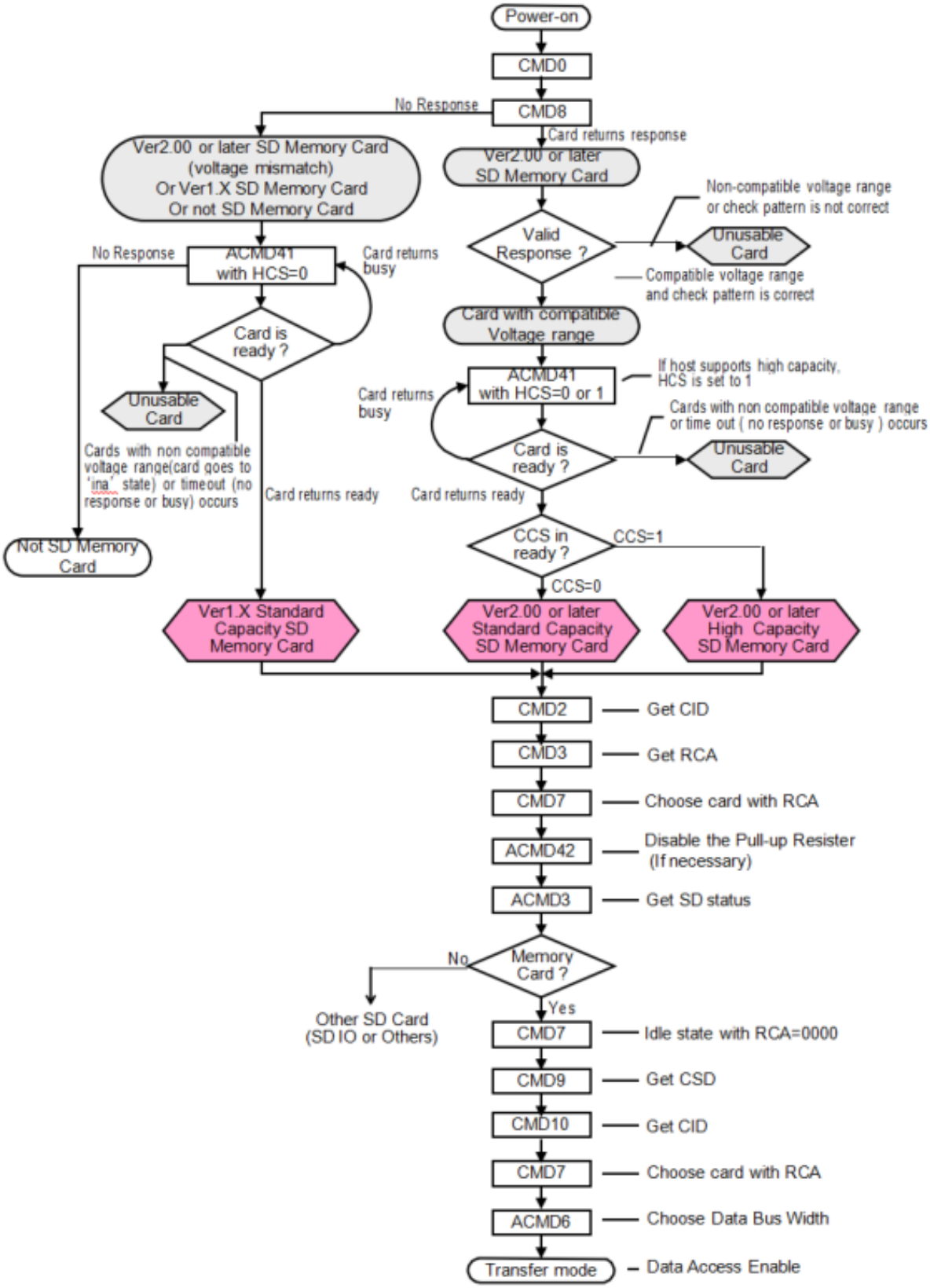


(*1) Note: Card returns busy when
- Card executes internal initialization process.
- If the card is High capacity SD Memory Card, there are 2 cases
  1. CMD8 was not issued before ACMD41
  2. ACMD41 is issued with HCS=0

(*2) Note: 2.1mm SD Memory Card can be initialized using CMD1 and Thin (1.4mm) SD Memory Card can be initialized using CMD1 only after firstly initialized by using CMD0 and ACMD41. In any of the cases CMD1 is not recommended because it may be difficult for the host to distinguish between MultiMediaCard and SD Memory Card.
If the SD card is initialized by CMD1 and the host treat it as MMC card, not SD card, the Data of the card may be damaged because of wrong interpretation of CSD and CID registers.

Card State Diagram (SPI mode)

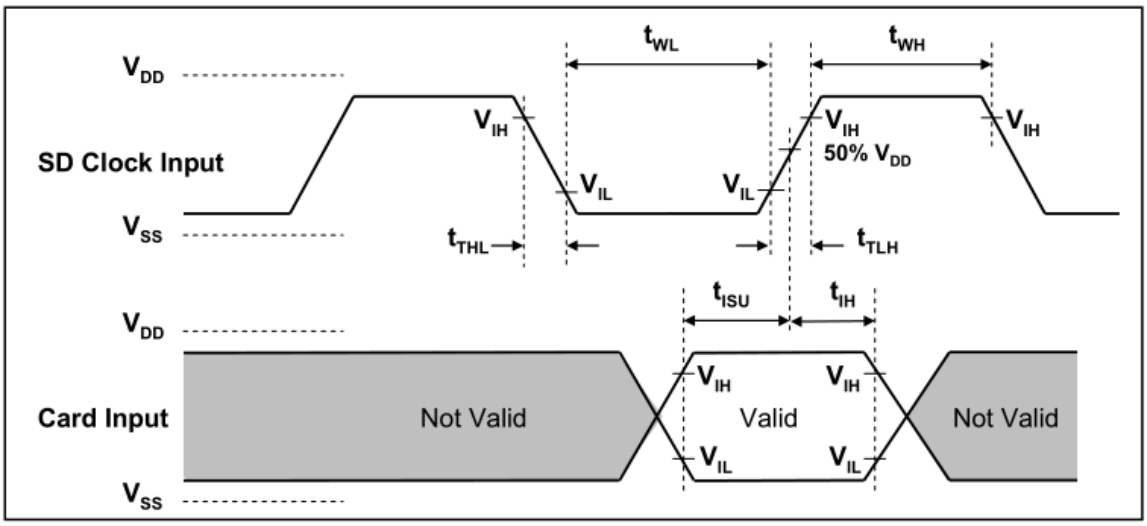
12. SD Mode


Power-on
CMD0
No Response
CMD8
Card returns response
Ver2.00 or later SD Memory Card (voltage mismatch) Or Ver1.X SD Memory Card Or not SD Memory Card
Ver2.00 or later SD Memory Card
Non-compatible voltage range or check pattern is not correct
Valid Response ?
Unusable Card
Compatible voltage range and check pattern is correct
No Response
ACMD41 with HCS=0
Card returns busy
Card is ready ?
Card with compatible Voltage range
If host supports high capacity, HCS is set to 1
ACMD41 with HCS=0 or 1
Card returns busy
Cards with non compatible voltage range or time out (no response or busy) occurs
Card is ready ?
Unusable Card
Unusable Card
Cards with non compatible voltage range(card goes to 'ina' state) or timeout (no response or busy) occurs
Card returns ready
Card returns ready
Not SD Memory Card
CCS in ready ?
CCS=1
CCS=0
Ver1.X Standard Capacity SD Memory Card
Ver2.00 or later Standard Capacity SD Memory Card
Ver2.00 or later High Capacity SD Memory Card
CMD2
Get CID
CMD3
Get RCA
CMD7
Choose card with RCA
ACMD42
Disable the Pull-up Resister (If necessary)
ACMD3
Get SD status
No
Memory Card ?
Yes
Other SD Card (SD IO or Others)
CMD7
Idle state with RCA=0000
CMD9
Get CSD
CMD10
Get CID
CMD7
Choose card with RCA
ACMD6
Choose Data Bus Width
Transfer mode
Data Access Enable

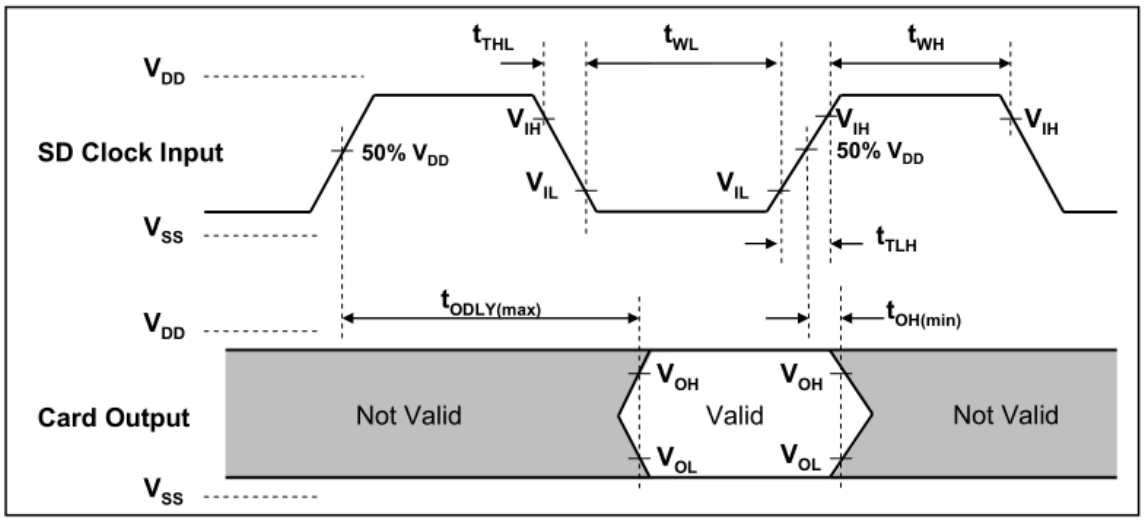
13. DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		VSS-0.3		0.25VCC	V
V_{IH}	Input high voltage		0.625VCC		VCC+0.3	V
V_{OL}	Output low voltage	IOL=100μA @VCC_min			0.125VCC	V
V_{OH}	Output high voltage	IOH=100μA @VCC_min	0.75VCC			V
I_{IN}	Input leakage current	VIN=VCC or 0	-10	+/-1	10	μA
I_{OUT}	Tri-state output leakage current		-10	+/-1	10	μA
I_{STBY}	Standby current	3.3V@clock stop		150	200	μA
I_{OP}	Operation current	3.3v@50MHz (Write)		15	25	mA
		3.3v@50MHz (Read)		15	25	mA

14. Bus Timing (High-Speed Mode)



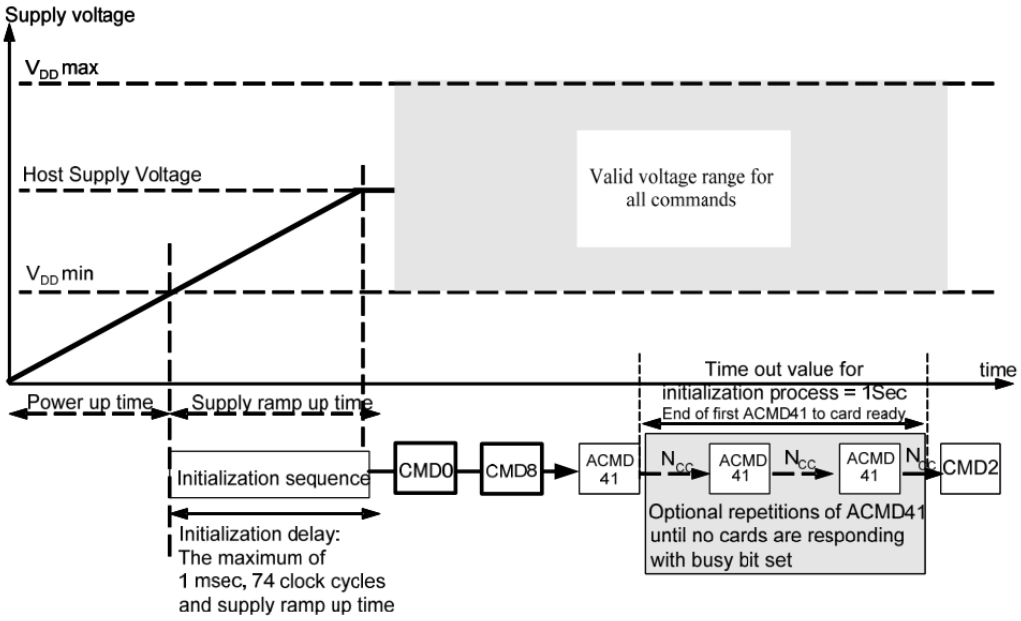
Card Input Timing (High Speed Card)



Card Output Timing (High Speed Mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10 pF (1 card)

15. Power Up



Power-up Diagram

'Power up time' is defined as voltage rising time from 0 volt to Vop min (refer to 6.6) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

'Supply ramp up time' provides the time that the power is built up to the operating level (Host Suppl Voltage) and the time to wait until the SD card can accept the first command.

The host shall supply power to the card so that the voltage is reached to Vdd min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPl mode, CS shall be held to high during 74 clock cycles.

After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. ln case of SD host, CMDO is not necessary. ln case of SPl host, CMDO shall be the first command to send the card to SPI mode.

CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up seauence, In case the host system connects multiple cards the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

Power Up Time